QKits TXRX24G transceiver module data sheet.

QUICK REFERENCE DATA

Parameter	Value	Unit
Minimum supply voltage	1.9	VDC
Maximum supply voltage	3.6	VDC
Maximum output power	0	dBm
Maximum data rate	1000	kbps
Supply current, transmit @ -5dBm output power	10.5	mA
Supply current in receive mode	18	mA
Temperature range	-40 to +85	°C
Sensitivity	-90	dBm
Supply current in Power Down mode	400	nA

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Features:

Data rate 0 to 1Mbps

Multi channel operation
- 125 channels
- Channel switching time <200ms.
- Support frequency hopping

Data slicer / clock recovery of data ·
· Address and CRC computation ·
· DuoCeiver™ for simultaneous dual receiver topology
· QBurst™ mode for ultra-low power operation and relaxed MCU performance

· Low supply current (TX), typical 10.5mA peak @ -5dBm output power
· Low supply current (RX), typical 18mA peak in receive mode
· 100 % RF tested

The transceiver consists of a fully integrated frequency synthesizer, a power amplifier, a crystal oscillator and a modulator. Output power and frequency channels are easily programmable by use of the 3-wire serial interface.

The TXRX24G can be set in the following main modes depending on three control pins:

Mode	PWR_UP	CE	CS
Active (RX/TX)	1	1	0
Configuration	1	0	1
Stand by	1	0	0
Power down	0	X	X

Pin assignments for TXRX24G:

CE - Digital Input, Chip Enable Activates RX or TX mode
CS - Digital Input, Chip Select Activates Configuration Mode

DR1 - Digital Output, RX Data Ready at Data Channel 1 (QBurst only)
DR2 - Digital Output, RX Data Ready at Data Channel 2 (QBurst only)

CLK1 Digital I/O Clock Input (TX) & Output/Input (RX) for Data Channel 1, 3-wire interface
CLK2 Digital I/O Clock Output/Input for RX Data Channel 2

DOUT2 Digital Output RX Data Channel 2
DATA Digital I/O RX Data Channel 1/TX Data Input/ 3-wire interface

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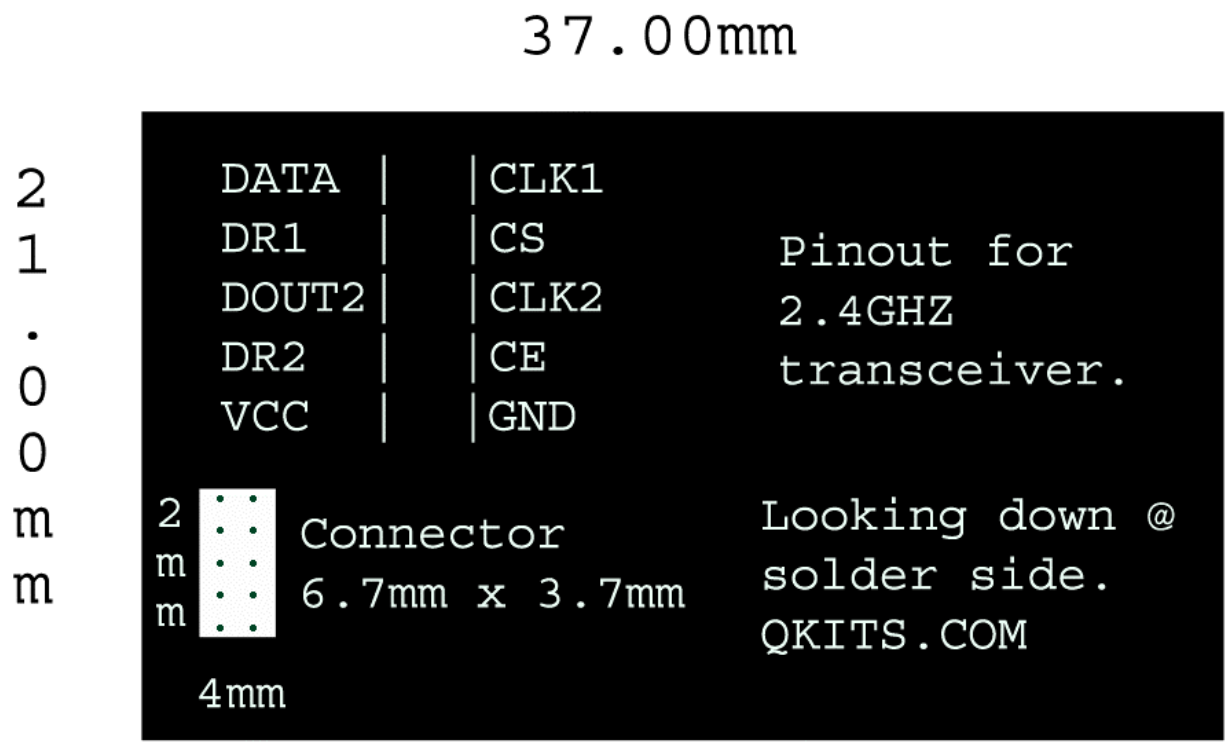


Active modes:
The TXRX24G has two active (RX/TX) modes:
- QBurst
- Direct Mode

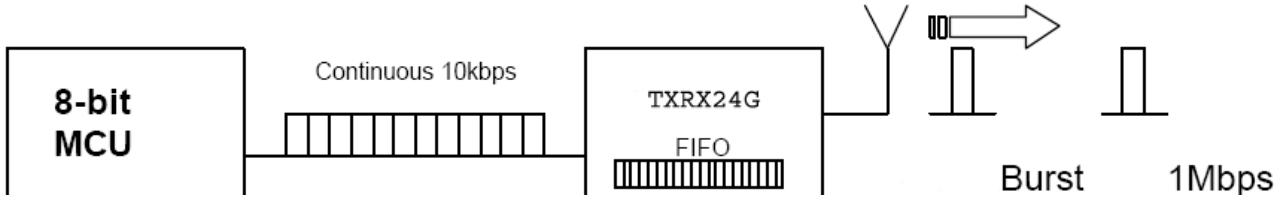
The device functionality in these modes is decided by the content of a configuration word. This configuration word is presented in configuration section.

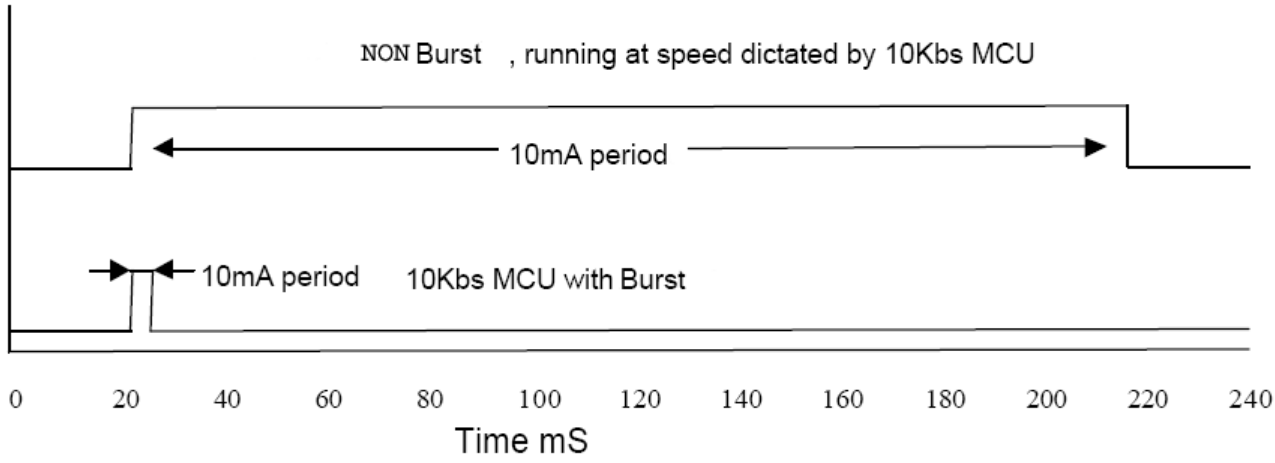
QBurst:
The QBurst technology uses on-chip FIFO to clock in data at a low data rate and transmit it at a very high rate thus enabling extreme power savings. When operating the TXRX24G in QBurst mode you gain access to the high data rates(1 Mbps) offered by the 2.4 GHz band without the need of a costly, high-speed micro controller (MCU) for data processing.
By putting all high speed signal processing related to RF protocol on the module offers the following benefits.
- Highly reduced current consumption
- Lower system cost (facilitates use of less expensive micro controller)
- Greatly **reduces** risk of 'on-air' collisions due to **short** transmission time

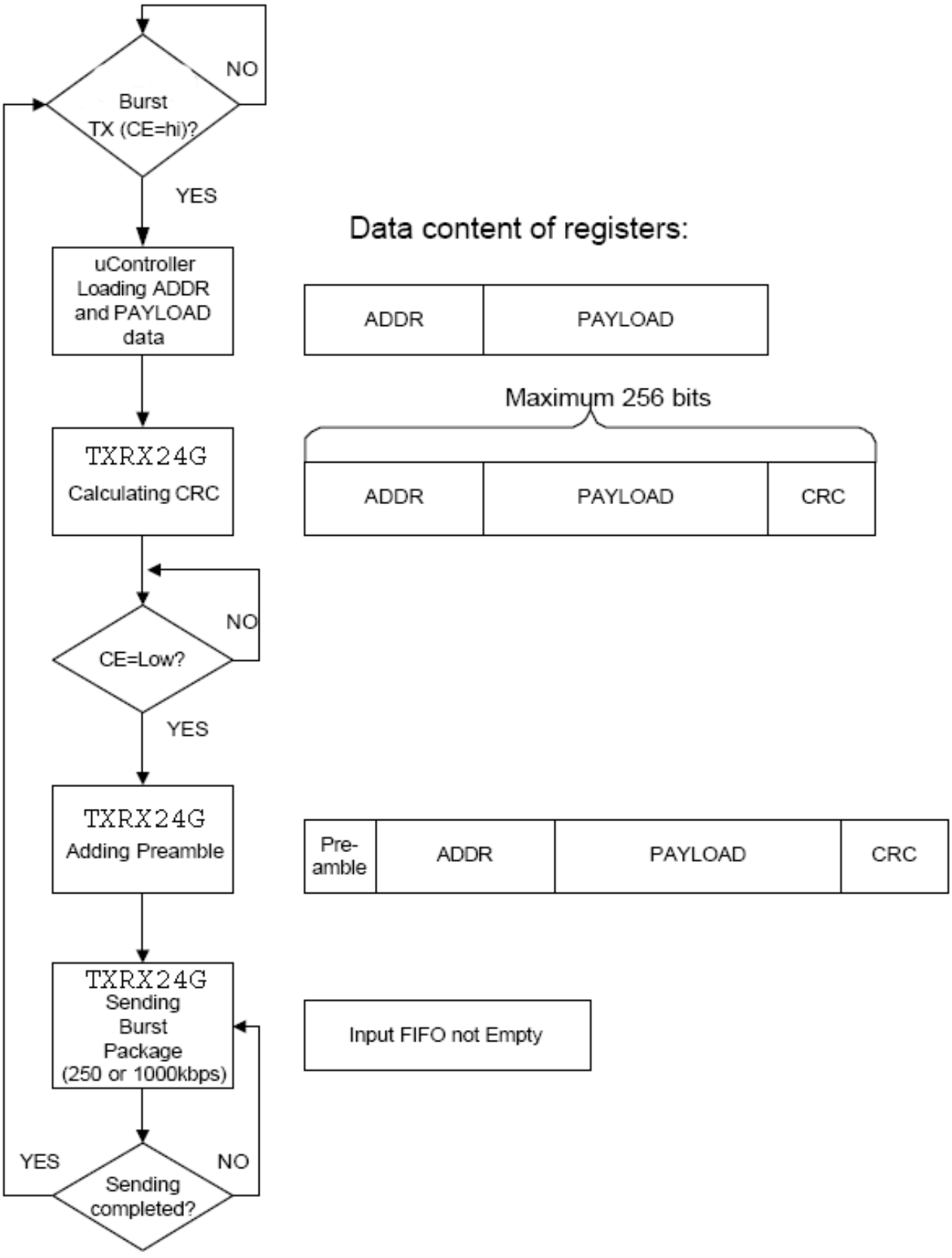
The TXRX24G can be programmed using a simple 3-wire interface where the data rate is decided by the speed of the micro controller. By allowing the digital part of the application to run at low speed while maximizing the data rate on the RF link, the QBurst mode reduces the average current consumption in applications considerably and greatly improves overall circuit reliability.

QBurst principle:

When the TXRX24G is configured in QBurst mode, TX or RX operation is conducted in the following way (10 kbps for the example only).




NON Burst , running at speed dictated by 10Kbs MCU
10mA period
10mA period
10Kbs MCU with Burst
0
20
40
60
80
100
120
140
160
180
200
220
240
Time mS



Sending data using the QBurst method.

MCU interface pins used: CE, CLK1, DATA

1. When the application MCU has data to send, set CE high. This activates TXRX24G on-board data processing.

2. The address of the receiving node (RX address) and payload data is clocked into the TXRX24G. The application protocol or MCU sets the speed <1Mbps (ex: 10kbps).

3. MCU sets CE low, this activates QBurst transmission.

4. The TXRX24G takes over and completes the process with the following steps:

   - RF front end is powered up
   - RF package is completed (preamble added, CRC calculated)
   - Data is transmitted at high speed (250 kbps or 1 Mbps configured by user).
   - TXRX24G returns to stand-by when finished.

   How simple is that.

To receive a QBurst transmission:

1. MCU interface pins used: CE, DR1, CLK1 and DATA (one RX channel receive)

2. Correct address and size of payload of incoming RF packages are set when TXRX24G is configured to QBurst RX.

3. To activate RX, set CE high.

4. After 200 μs settling, the TXRX24G begins monitoring the air ways for incoming communication.

5. When a valid package has been received (correct address and CRC found),TXRX24G removes the preamble, address and CRC bits.

6. TXRX24G then notifies (interrupts) the MCU by setting the DR1 pin high.

7. MCU may (or may not) set the CE low to disable the RF front end (low current mode).

8. The MCU will clock out just the payload data at a suitable rate (ex. 10 kbps).

9. When all payload data is retrieved the TXRX24G sets DR1 low again, and is ready for new incoming data package if CE is kept high during data download. If the CE was set low, a new start up sequence can begin.

Direct Mode:

In direct mode the TXRX24G works like a traditional RF device. Data must be at 1Mbps ±200ppm, or 250kbps ±200ppm at low data rate setting, for the receiver to detect the signals.

MCU interface pins used: CE, DATA

1. When application MCU has data to send, set CE high.
2. The TXRX24G RF front end is now immediately activated, and after 200 μs settling time, data will modulate the carrier directly.
3. All RF protocol parts must hence be implemented in MCU firmware (preamble, address and CRC).

Direct Mode Receive:

MCU interface pins used: CE, CLK1, and DATA

1. Once the TXRX24G is configured and powered up (CE high) in direct RX mode, DATA will start to toggle due to noise present on the air.
2. CLK1 will also start to toggle as TXRX24G is trying to lock on to the incoming data stream.
3. Once a valid preamble arrives, CLK1 and DATA will lock on to the incoming signal and the RF package will appear at the DATA pin with the same speed as it is transmitted.
4. To enable the demodulator to re-generate the clock, the preamble must be 8 bits toggling hi-low, starting with low if the first data bit is low.
5. In this mode no data ready (DR) signals is available. Address and checksum verification must also be done in the receiving MCU.

Simultaneous Two Channel Receive Mode:

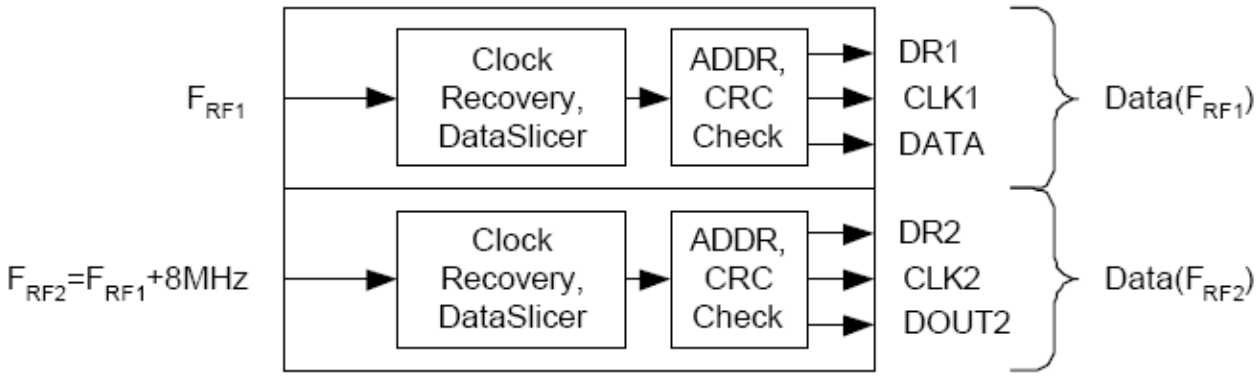
In both QBurst & direct modes the TXRX24G can facilitate simultaneous reception of two parallel independent frequency channels at the maximum data rate.

This means:

• TXRX24G can receive data from two 1 Mbps transmitters (ex: TXRX24G 8 MHz (8 frequency channels) apart through one antenna interface.
• The output from the two data channels is fed to two separate MCU interfaces.
• Data channel 1: CLK1, DATA, and DR1
• Data channel 2: CLK2, DOUT2, and DR2
• DR1 and DR2 are available only in QBurst mode
.

The TXRX24G dual receiver technology provides 2 separate dedicated data channels for RX and replaces the need for two, stand alone receiver systems.

There is one absolute requirement for using the second data channel. For theTXRX24G to be able to receive at the second data channel the frequency channel must be 8MHz higher than the frequency of data channel 1. The TXRX24G must be programmed to receive at the frequency of data channel 1. No time multiplexing is used in TXRX24G to fulfill this function. In direct mode the MCU must be able to handle two simultaneously incoming data packets if it is not multiplexing between the two data channels. In QBurst it is possible for the MCU to clock out one data channel at
a time while data on the other data channel waits for MCU availability, without any lost data packets, and by doing so reduce the needed performance of the MCU.



Configuration Mode:

In configuration mode a configuration word of up to 15 bytes is downloaded to TXRX24G. This is done through a simple 3-wire interface (CS, CLK1 and DATA).

Stand-By Mode:

Stand by mode is used to minimize average current consumption while maintaining short start up times. In this mode, part of the crystal oscillator is active. Current consumption is dependent on crystal frequency (Ex: 32 μA @ 16 MHz TXRX24G crystal). The configuration word content is maintained during stand by.

Power Down Mode:

In power down the TXRX24G is disabled with minimal current consumption, typically less than 1μA. Entering this mode when the device is not active minimizes average current consumption, maximizing battery lifetime. The configuration word content is maintained during power down.

Pin configuration for the different modes of the TXRX24G:

TXRX24G	MODE SWITCHES		INPUT PINS			BIDIR PINS			OUTPUT PINS		
MODES						direction	direction	direction			
	RXMODE	QBurst	PWR_UP	CE	CS	CLK1	DATA	CLK2	DR1	DR2	DOUT2
Power down	X	X	0	X[1]	1	In X	In X	In X	0	0	0
						In	In	In			
Power down	0	1	0	X	0	X	X	X	0	0	0
Power down	1	1	0	X	0	In CLK	In X	In X	0	0	0
Stand by	0	X	1	0	0	In X	In X	In X	0	0	0
Stand by	1	0	1	0	0	In X	In X	In X	0	0	0
Stand by	1	1	1	0	0	In CLK	In[2] DATA	In X	0	DR2	0
Stand by	1	1	1	0	0	In CLK	Out[3] DATA	In X	1	DR2	0
Configuration	X	X	1	0	1	In CLK	In CONFIG DATA	In X	0	0	0
TX QBurst™	0	1	1	1	0	In CLK	In DATA	In X	0	0	0
TX Direct	0	0	1	1	0	In X	In DATA	In X	0	0	0
RX QBurst™ in one channel	1	1	1	1	0	In CLK	Out DATA	In X	DR1	0	0
RX QBurst™ in two channels	1	1	1	1	0	In CLK	Out DATA	In CLK	DR1	DR2	DATA
RX Direct in one channel	1	0	1	1	0	Out CLK	Out DATA	Out 0	0	0	0
RX Direct in two channels	1	0	1	1	0	Out CLK	Out DATA	Out CLK	0	0	DATA

1 In = X means the input should be set to either “low” or “high”.
2 Input if DR1 is “low”.
3 Output if DR1 is “high”

DEVICE CONFIGURATION:

All configuration of the TXRX24G is done via a 3-wire interface to a single configuration register. The configuration word can be up to 15 bytes long for QBurst use and up to 2 bytes long for direct mode.

Configuration for QBurst operation:

The configuration word in QBurst enables the TXRX24G to handle the RF protocol. Once the protocol is completed and loaded into TXRX24G only one byte, bit[7:0], needs to be updated during actual operation.

The configuration blocks dedicated to QBurst is as follows:

- Payload section width: Specifies the number of payload bits in a RF package.

This enables the TXRX24G to distinguish between payload data and the CRC bytes in a received package.

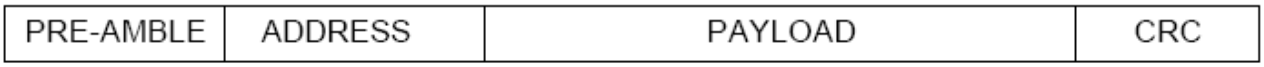
- Address width: Sets the number of bits used for address in the RF package. This enables the TXRX24G to distinguish between address and payload data.

- Address (RX Channel 1 and 2): Destination address for received data.

- CRC: Enables TXRX24G on-chip CRC generation and de-coding.

NOTE:

These configuration blocks, with the exception of the CRC, are dedicated for the packages that a TXRX24G is to receive. In TX mode, the MCU must generate an address and a payload section that fits the configuration of the TXRX24G that is to receive the data. When using the TXRX24G on-chip CRC feature ensure that CRC is enabled and uses the same length for both the TX and RX devices.



Configuration for Direct Mode operation:

For direct mode operation only the two first bytes (bit[15:0]) of the configuring word are relevant.

Configuration Word overview:

	Bit position	Number of bits	Name	Function
QBurst configuration	143:120	24	TEST	Reserved for testing
	119:112	8	DATA2_W	Length of data payload section RX channel 2
	111:104	8	DATA1_W	Length of data payload section RX channel 1
	103:64	40	ADDR2	Up to 5 byte address for RX channel 2
	63:24	40	ADDR1	Up to 5 byte address for RX channel 1
	23:18	6	ADDR_W	Number of address bits (both RX channels).
	17	1	CRC_L	8 or 16 bit CRC
	16	1	CRC_EN	Enable on-chip CRC generation/checking.
General device configuration	15	1	RX2_EN	Enable two channel receive mode
	14	1	CM	Communication mode (Direct or QBurst)
	13	1	RFDR_SB	RF data rate (1Mbps requires 16MHz crystal)
	12:10	3	XO_F	Crystal frequency
	9:8	2	RF_PWR	RF output power
	7:1	7	RF_CH#	Frequency channel
	0	1	RXEN	RX or TX operation

The configuration word is shifted in MSB first on positive CLK1 edges. New configuration is enabled on the falling edge of CS.

NOTE. On the falling edge of CS, the TXRX24G updates the number of bits actually shifted in during the last configuration. Ex: If the TXRX24G is to be configured for 2 channel RX in QBurst a total of 120 bits must be shifted in during the first configuration after VDD is applied. Once the wanted protocol, modus and RF channel are set, only one bit (RXEN) is shifted in to switch between RX and TX.

Configuration Word Detailed Description bit by bit:

The following describes the function of the 144 bits (bit 143 = MSB) that is used to configure the TXRX24G.

General Device Configuration: bit[15:0]
QBurst Configuration: bit[119:16]
Test Configuration: bit[143:120]

MSB	TEST						
D143	D142	D141	D140	D139	D138	D137	D136
Reserved for testing							
1	0	0	0	1	1	1	0 Default

MSB	TEST													
D135	D134	D133	D132	D131	D130	D129	D128	D127	D126	D125	D124	D123	D122	D121	D120
Reserved for testing														Close PLL in TX	
0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0 Default

DATA2_W							
D119	D118	D117	D116	D115	D114	D113	D112
Data width channel#2 in # of bits excluding addr/crc							
0	0	1	0	0	0	0	0 Default

DATA1_W							
D111	D110	D109	D108	D107	D106	D105	D104
Data width channel#1 in # of bits excluding addr/crc							
0	0	1	0	0	0	0	0 Default

ADDR2											
D103	D102	D101	….	D71	D70	D69	D68	D67	D66	D65	D64
Channel#2 Address RX (up to 40bit)											
0	0	0	…	1	1	1	0	0	1	1	1 Default

ADDR1											
D63	D62	D61	….	D31	D30	D29	D28	D27	D26	D25	D24
Channel#1 Address RX (up to 40bit)											
0	0	0	…	1	1	1	0	0	1	1	1 Default

ADDR_W						
D23	D22	D21	D20	D19	D18	
Address width in # of bits (both channels)						
0	0	1	0	0	0	Default

CRC		
D17	D16	
CRC Mode 1 = 16bit, 0 = 8bit	CRC 1 = enable; 0 = disable	
0	1	Default

RF-Programming															LSB	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Two Ch.	BUF	OD	XO Frequency			RF Power		Channel selection							RXEN	
0	0	0	0	1	1	1	1	0	0	0	0	0	1	0	0	Default

The MSB bit should be loaded first into the configuration register.

Default configuration word: h 0x8E08.1C20.2000.0000.00E7.0000.0000.E721.0F04.

QBurst configuration:

The section bit[119:16] contains the segments of the configuration register dedicated to QBurst™ operational protocol. After VDD is turned on QBurst™ configuration is done once and remains set whilst VDD is present. During operation only the first byte for frequency channel and RX/TX switching need to be changed.

PLL_CTRL:

PLL_CTRL		
D121	**D120**	**PLL**
0	0	Open TX/Closed RX
0	1	Open TX/Open RX
1	0	Closed TX/Closed RX
1	1	Closed TX/Open RX

Bit **121-120**:

PLL_CTRL: Controls the setting of the PLL for test purposes. With closed PLL in TX no deviation will be present. For normal operational mode these two bits must both be low.

DATAx_W

DATA2_W							
119	118	117	116	115	114	113	112

DATA1_W							
111	110	109	108	107	106	105	104

Number of bits in payload.

Bit **119 – 112**:

DATA2_W: Length of RF package payload section for receive-channel 2.

Bit **111 – 104**:

DATA1_W: Length of RF package payload section for receive-channel 1.

NOTE:The total number of bits in a QBurst™ RF package may not exceed 256!
Maximum length of payload section is hence given by:

$$DATAx\_W(bits) = 256 - ADDR\_W - CRC$$

Where:

ADDR_W: length of RX address set in configuration word B[23:18]
CRC: check sum, 8 or 16 bits set in configuration word B[17]
PRE: preamble, 8 bits are automatically included

Shorter address and CRC leaves more room for payload data in each package.

ADDRx

ADDR2											
103	102	101	….	71	70	69	68	67	66	65	64

ADDR1											
63	62	61	….	31	30	29	28	27	26	25	24

Address of receiver #2 and receiver #1.

Bit **103 – 64**:

ADDR2: Receiver address channel 2, up to 40 bit.

Bit **63 – 24**: ADDR1

ADDR1: Receiver address channel 1, up to 40 bit.

NOTE!

Bits in ADDRx exceeding the address width set in ADDR_W are redundant and can be set to logic 0.

ADDR_W & CRC

ADDR_W						CRC_L	CRC_EN
23	22	21	20	19	18	17	16

Number of bits reserved for RX address + CRC setting.

Bit **23 – 18**:

ADDR_W: Number of bits reserved for RX address in QBurst™ packages.

NOTE: Maximum number of address bits is 40 (5 bytes). Values over 40 in ADDR_W are not valid.

Bit **17**:

CRC_L: CRC length to be calculated by TXRX24G in QBurst™.
Logic 0: 8 bit CRC
Logic 1: 16 bit CRC

Bit: **16**:

CRC_EN: Enables on-chip CRC generation (TX) and verification (RX).
Logic 0: On-chip CRC generation/checking disabled
Logic 1: On-chip CRC generation/checking enabled

NOTE: An 8 bit CRC will increase the number of payload bits possible in each QBurst™ data packet, but will also reduce the system integrity.

General device configuration:

This section of the configuration word handles RF and device related parameters.

Modes:

RX2_EN	CM	RFDR_SB	XO_F			RF_PWR	
15	14	13	12	11	10	9	8

RF operational settings.

Bit **15**:

RX2_EN:
Logic 0: One channel receive
Logic 1: Two channels receive

NOTE: In two channels receive, the TXRX24G receives on two, separate frequency channels simultaneously. The frequency of receive channel 1 is set in the configuration word bit[7-1], receive channel 2 is always 8 channels (8 MHz) above receive channel 1.

Bit **14**:

Communication Mode:
Logic 0: TXRX24G operates in direct mode.
Logic 1: TXRX24G operates in QBurst™ mode

Bit **13**:

RF Data Rate:
Logic 0: 250 kbps
Logic 1: 1 Mbps

NOTE: Utilizing 250 kbps instead of 1Mbps will improve the receiver sensitivity by 10 dB. 1Mbps requires 16MHz crystal which is what the TXRX24G uses.

Bit **12-10**:

XO_F: Selects the TXRX24G crystal frequency to be used:

XO FREQUENCY SELECTION			
D12	**D11**	**D10**	**Crystal Frequency [MHz]**
0	0	0	4
0	0	1	8
0	1	0	12
0	1	1	16
1	0	0	20

Crystal frequency setting.

TXRX24G uses a 16 MHz crystal.

Bit **9-8**:

RF_PWR: Sets TXRX24G RF output power in transmit mode:

RF OUTPUT POWER		
D9	**D8**	**P [dBm]**
0	0	-20
0	1	-10
1	0	-5
1	1	0

RF output power setting.

RF channel & direction

RF_CH#							**RXEN**
7	6	5	4	3	2	1	0

Frequency channel and RX / TX setting.

Bit **7 – 1**:

RF_CH#: Sets the frequency channel the TXRX24G operates on.

The channel frequency in ***transmit*** is given by:

$Channel_{RF} = 2400\ MHz + RF\_CH$ #1.0MHz

RF_CH #: between 2400MHz and 2527MHz may be set.

The channel frequency in ***data channel 1*** is given by:

$Channel_{RF}$ 0 . 1 # _ 2400 · + = (Receive at PIN#8)

RF_CH #: between 2400MHz and 2524MHz may be set.

NOTE: The channels above 83 can only be utilized in certain territories (ex: Japan)

The channel frequency in ***data channel 2*** is given by:

$Channel_{RF}$ 0 . 1 # _ 2400 · + = +8MHz (Receive at PIN#4)

RF_CH #: between 2408MHz and 2524MHz may be set.

Bit **0**:

Set active mode:

Logic 0: transmit mode

Logic 1: receive mode

DATA PACKAGE DESCRIPTION

Data Package Diagram

The data packet for both QBurst™ mode and direct mode communication is divided into 4 sections. These are:

1. PREAMBLE	• The preamble field is required in QBurst™ and Direct modes. • Preamble is 8 bits in length and is dependent of the first data bit in direct mode. PREAMBLE 1stADDR-BIT 01010101 0 10101010 1 • Preamble is automatically added to the data packet in QBurst™ and thereby gives extra space for payload. In Direct mode MCU must handle preamble. In QBurst™ mode RX, the preamble is removed from the received output data, in direct mode the preamble is transparent to the output data.
2 ADDRESS	• The address field is required in QBurst™ mode.[1] • 8 to 40 bits length. • Address automatically removed from received packet in QBurst™ mode. In Direct mode MCU must handle address.
3 PAYLOAD	• The data to be transmitted • In QBurst™ mode payload size is 256 bits minus the following: (Address: 8 to 40 bits. + CRC 8 or 16 bits). • In Direct mode the maximum packet size (length) is for 1Mbps 4000 bits (4ms).
4 CRC	• The CRC is optional in QBurst™ mode, and is not used in Direct mode. • 8 or 16 bits length • The CRC is removed from the received output data in QBurst™ RX.

Data package description

[1] Suggestions for the use of addresses in QBurst™: In general more bits in the address gives less false detection, which in the end may give lower data packet loss.
A. The address made by (5, 4, 3, or 2) equal bytes are not recommended because it in general will make the packet-error-rate increase.
B. Addresses where the level shift only one time (i.e. 000FFFFFFF) could often be detected in noise that may give a false detection, which again may give raised packet-error-rate.
Direct mode will be dependent on the software used in the MCU, but it is recommended to have the same restrictions on addresses for this mode.

IMPORTANT TIMING DATA

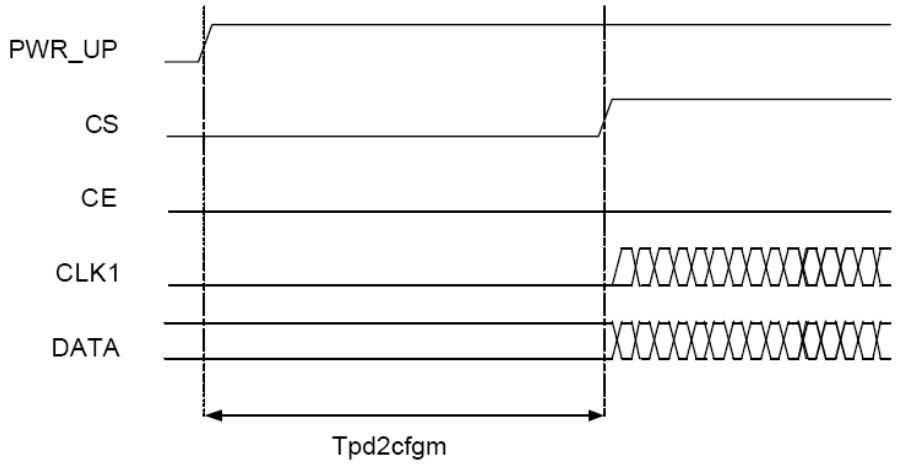
The following timing applies for operation of TXRX24G.

TXRX24G Timing Information

TXRX24G timing	Max.	Min.	Name
PWR_DWN ⓾ Configuration mode	3ms		Tpd2cfgm
PWR_DWN➔ Active mode (RX/TX)	3ms		Tpd2a
ST_BY ➔ TX QBurst™	195µs		Tsby2txSB
ST_BY ➔ TX Direct Mode	202µs		Tsby2txDM
ST_BY ➔ RX mode	202µs		Tsby2rx
Minimum delay from CS to data.		5µs	Tcs2data
Minimum delay from CE to data.		5µs	Tce2data
Minimum delay from DR1/2 to clk.		50ns	Tdr2clk
Maximum delay from clk to data.	50ns		Tclk2data
Delay between edges		50ns	Td
Setup time		500ns	Ts
Hold time		500ns	Th
Delay to finish internal GFSK data		1/data rate	Tfd
Minimum input clock high		500ns	Thmin
Set-up of data in Direct Mode	50ns		Tsdm
Minimum clock high in Direct Mode		300ns	Thdm
Minimum clock low in Direct Mode		230ns	Tldm
Time on air, TX Direct mode	4ms		ToaDM

Operational timing of TXRX24G

When the TXRX24G is in power down it must always settle in stand by for 3ms before it can enter configuration or one of the active modes.



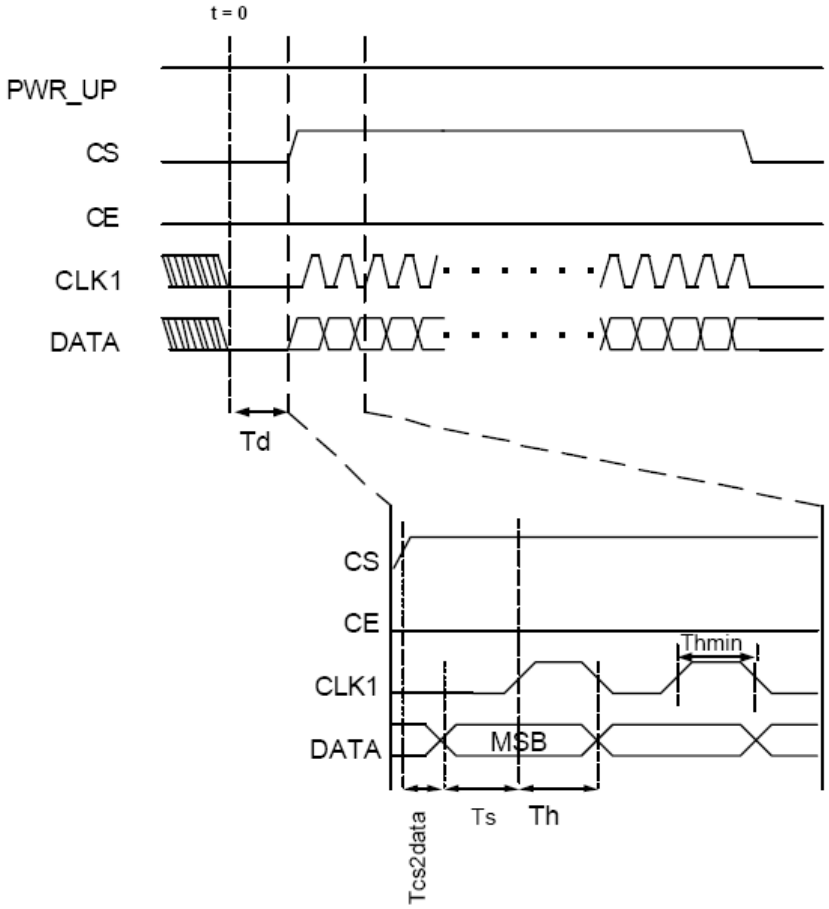
Timing diagram for power down (or VDD off) to configuration mode for TXRX24G.

Note: The configuration word will be lost when VDD is turned off and that the device then must be configured before going to one of the active modes. If the device is configured one can go directly from power down to the wanted active mode.

Note: CE and CS may not be high at the same time. Setting one or the other decides whether configuration or active mode is entered.

Configuration mode timing:

When one or more of the bits in the configuration word needs to be changed the following timing sequences apply.

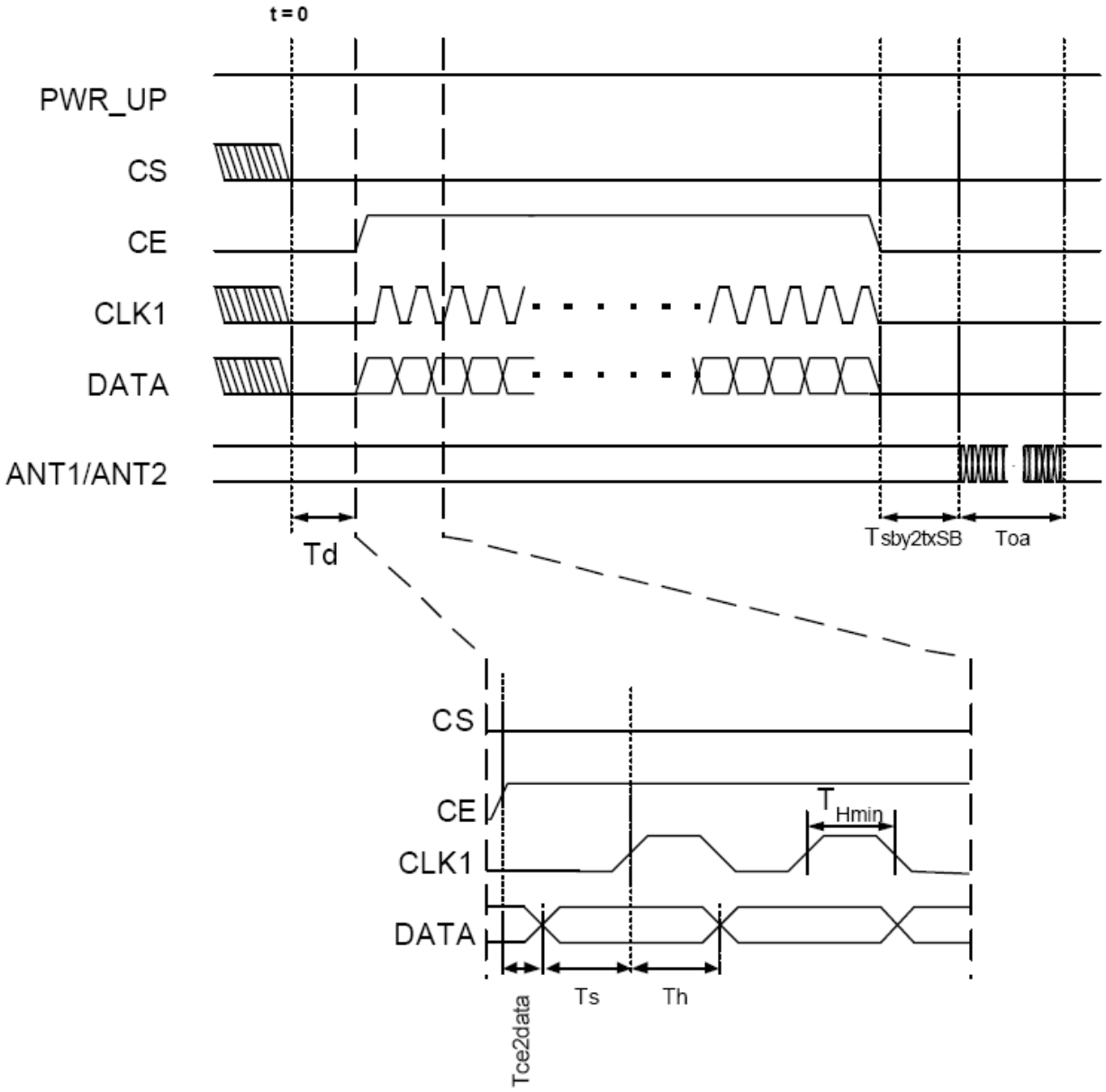


Timing diagram for configuration.

If configuration mode is entered from power down, CS can be set high after Tpd2sby.

QBurst™ Mode timing

QBurst™ TX:

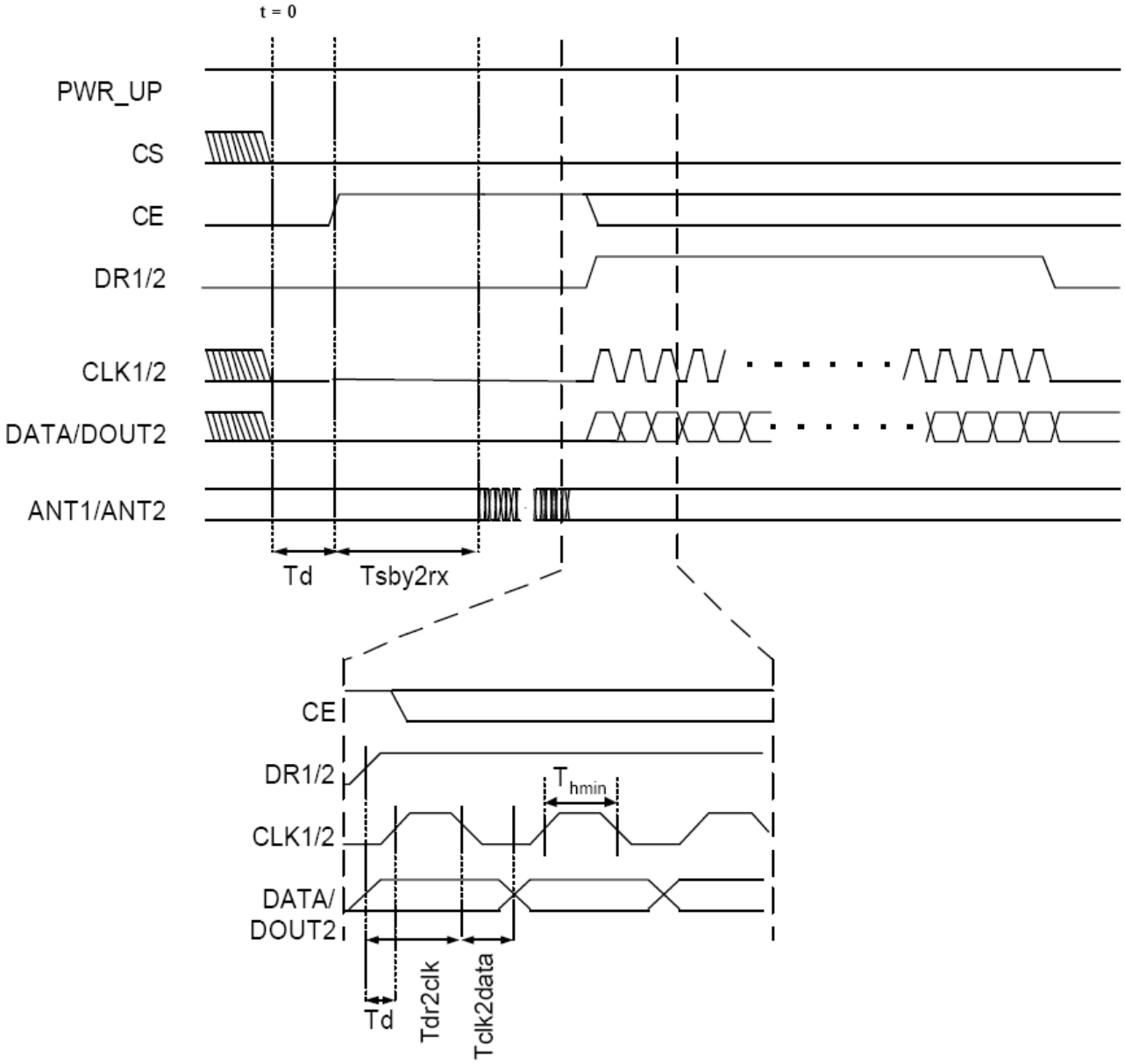


Timing of QBurst™ in TX

The package length and the data rate give the delay Toa (time on air), as shown in the equation.

$$\textbf{\textit{Toa=1}} \,/\, \textit{datarate} \cdot (\#\textit{databits}+1)$$

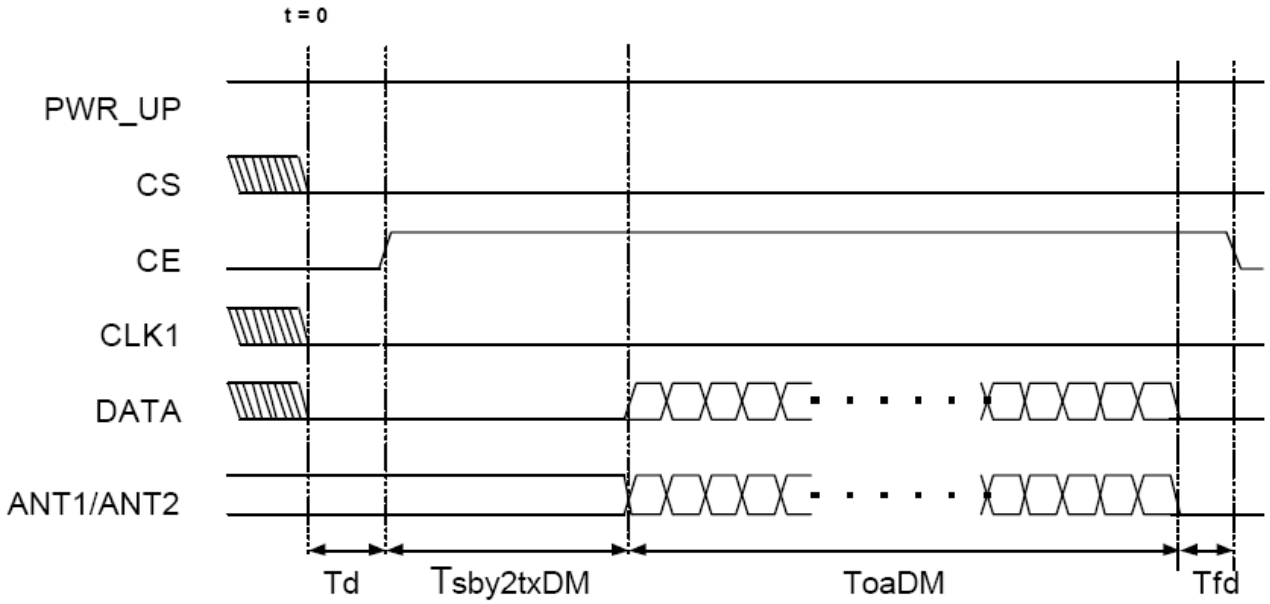
QBurst™ RX:



Timing of QBurst™ in RX

The CE may be kept high during downloading of data, but the cost is higher current consumption (18mA) and the benefit is short start-up time (200µs) when DR1 goes low.

Direct Mode
Direct Mode TX:



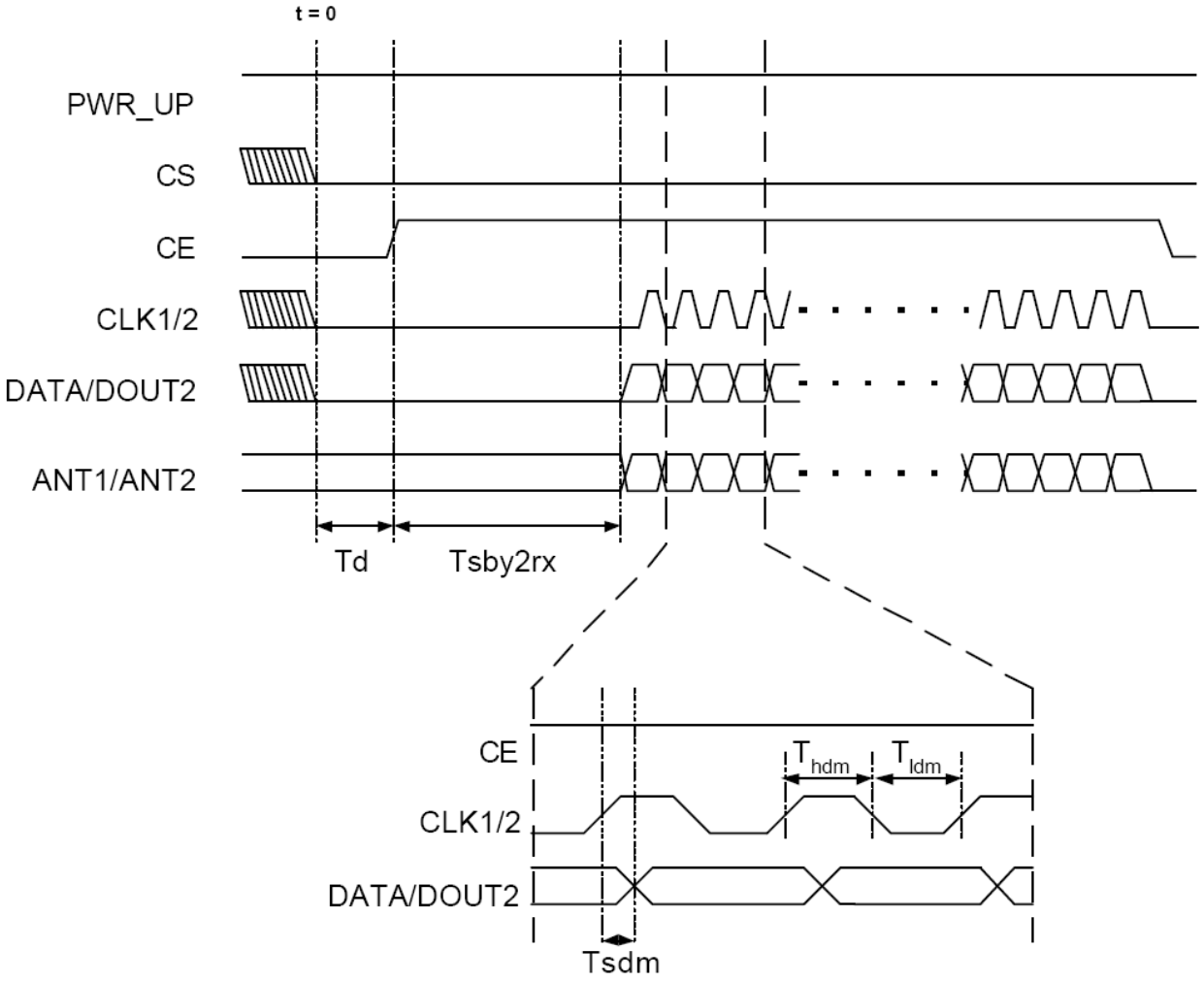
Timing of direct mode TX

In TX direct mode the input data will be sampled by TXRX24G and therefore no clock is needed. The clock must be stable at low level during transmission due to noise considerations. The exact delay $T_{sby2txDM}$ is given by the equation:

$$T_{sby2txDM} = 194us + 1/F_{XO} \cdot 14 + 2.25us$$

The maximum length of a package (ToaDM) over all voltages and temperatures is 4ms. This is limited by frequency drift in the transmitter and is independent of data rate and frequency channel.

Direct Mode RX:



Timing of direct mode RX

Tsby2rx describes the delay from the positive edge of CE to start detection of (demodulating) incoming data.

PERIPHERAL RF INFORMATION

Antenna output

The ANT1 & ANT2 output pins provide a balanced RF output to the antenna. The pins must have a DC path to VDD, either via a RF choke or via the center point in a dipole antenna. The load impedance seen between the ANT1/ANT2 outputs should be in the range 200-700Ω. A load of 100Ω+j175Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network.

Output Power adjustment

Power setting bits of configuring word	RF output power	DC current consumption
11	0 dBm ±3dB	13.0 mA
10	-5 dBm ±3dB	10.5 mA
01	-10 dBm ±3dB	9.4 mA
00	-20 dBm ±3dB	8.8 mA

Conditions: VDD = 3.0V, VSS = 0V, TA = 27ºC, Load impedance = 100Ω+j175Ω.

RF output power setting for the TXRX24G.